LISTING OF THE CLAIMS:

Claim 1 (Original) A method for forming an integrated circuit on a final substrate comprising the steps of:

selecting a first substrate including a base substrate and an at least partially crystalline porous release layer;

forming a semiconductor layer on said porous release layer on said first substrate, said semiconductor layer having a bottom surface in contact with said porous release layer and an upper surface;

forming at least one semiconductor device in said upper surface of said semiconductor layer;

bonding said upper surface of said semiconductor layer to a temporary auxiliary substrate;

detaching said semiconductor layer from said first substrate by breaking apart said porous release layer;

bonding said bottom surface of said semiconductor layer to a final substrate; and

detaching said semiconductor layer from said temporary auxiliary substrate.

Claim 2 (Original) The method of claim 1 wherein said step of bonding to said temporary auxiliary substrate includes the step of forming an adhesive layer.

Claim 3 (Original) The method of claim 1 wherein said step of bonding to said final substrate includes the step of forming an adhesive layer.

Claim 4 (Original) The method of claim 1 wherein said at least one semiconductor device is selected from the group consisting of n-type metal-oxide-semiconductor device (NMOS), p-type MOS (PMOS) devices, complementary MOS (CMOS) devices, bipolar transistors, bipolar and CMOS (BiCMOS) devices.

Claim 5 (Original) The method of claim 1 wherein said step of forming at least one semiconductor device further includes the step of forming insulating regions extending through said semiconductor layer.

Claim 6 (Original) The method of claim 1 wherein said semiconductor layer containing at least one semiconductor device further includes additional layers containing interconnection circuitry.

Claim 7 (Original) The method of claim 1 wherein said semiconducting layer is selected from the group consisting of silicon, silicon-germanium alloys, silicon-carbon alloys, silicon-germanium alloys containing carbon; the aforementioned materials doped with any element; the aforementioned materials in layered or graded composition combinations; the aforementioned materials in single crystal, polycrystalline, or nanocrystalline form.

Claim 8 (Original) The method of claim 1 wherein said semiconductor layer has a thickness in the range from 20 to 1000 nm.

Claim 9 (Original) The method of claim 1 wherein said final substrate further includes the step of forming one of passive cooling and active cooling.

Claim 10 (Original) The method for claim 1 wherein said final substrate is selected from the group consisting of single crystal silicon, diamond, quartz, crystalline oxides, crystalline or amorphous nitrides, amorphous or glassy oxides, plastics, and organic-inorganic composites.

Claim 11 (Original) The method of claim 1 wherein said final substrate comprises a base substrate with one or more overlayers selected from the group consisting of highly insulating (>1 kΩ-cm) single-crystal Si, highly insulating (>1 kΩ-cm) single-crystal silicon germanium, highly insulating (>1 kΩ-cm) polycrystalline Si or highly insulating (>1 kΩ-cm) polycrystalline silicon germanium, single crystal diamond, polycrystalline diamond; silicon oxide; aluminum oxide, other metal oxides, aluminum nitride, other crystalline or amorphous nitrides, and mixtures thereof.

Claim 12 (Original) The method of claim 11 wherein said base substrate is selected from the group consisting of single crystal silicon, diamond, crystalline oxides, crystalline or amorphous nitrides, amorphous or glassy oxides, plastics, and organic-inorganic composites.

Claim 13 (Original) The method of claim 1 wherein said at least partially crystalline porous layer is selected from the group consisting of at least one porous

silicon germanium alloy layer ($Si_{1-x}Ge_x$, where $0<x<1$ and x may be constant or spatially variable) and at least one porous silicon germanium alloy layer in combination with porous Si.

Claim 14 (Original) A method for forming an integrated circuit on a final substrate comprising the steps of:

forming a semiconductor layer on a first substrate, said first substrate comprising a base substrate and an at least partially crystalline porous release layer;

processing said semiconductor layer to form at least one semiconductor device;

bonding said semiconductor layer to a final substrate; and

detaching said semiconductor layer form said first substrate by breaking apart said porous release layer.

Claim 15 (Original) The method of claim 14 wherein said step of bonding to said final substrate includes the step of forming an adhesive layer.

Claim 16 (Original) The method of claim 14 wherein said at least one semiconductor device is selected from the group consisting of n-type metal-oxide-semiconductor devices (NMOS), p-type MOS (PMOS) devices, complementary MOS (CMOS) devices, bipolar transistors, bipolar and CMOS (BiCMOS) devices.

Claim 17 (Original) The method of claim 1 wherein said step of forming at least one semiconductor device further includes the step of forming insulating regions extending through said semiconductor layer.

Claim 18 (Original) The method of claim 14 wherein said semiconductor layer containing at least one semiconductor device further includes additional layers containing interconnection circuitry.

Claim 19 (Original) The method of claim 14 wherein said semiconducting layer is selected from the group consisting of silicon, silicon-germanium alloys, silicon-carbon alloys, silicon-germanium alloys containing carbon; the aforementioned materials doped with any element; the aforementioned materials in layered or graded composition combinations; the aforementioned materials in single crystal, polycrystalline, or nanocrystalline form.

Claim 20 (Original) The method of claim 14 wherein said semiconductor layer has a thickness in the range from 20 to 1000 nm.

Claim 21 (Original) The method of claim 14 wherein said final substrate further includes the step of forming one of passive cooing and active cooling.

Claim 22 (Original) The method of claim 14 wherein said final substrate is selected from the group consisting of single crystal silicon, diamond, quartz, crystalline

oxides, crystalline or amorphous nitrides amorphous or glassy oxides, plastics, and organic-inorganic composites.

Claim 23 (Original) The method of claim 14 wherein said final substrate comprises a base substrate with one or more overlayers selected from the group consisting of highly insulating (>1 kΩ-cm) single-crystal Si, highly insulating (>1 kΩ-cm) single-crystal silicon germanium, highly insulating (>1 kΩ-cm) polycrystalline Si or highly insulating (>1 kΩ-cm) polycrystalline silicon germanium, single crystal diamond, polycrystalline diamond; silicon oxide; aluminum oxide, other metal oxides, aluminum nitride, other crystalline or amorphous nitrides, and mixtures thereof.

Claim 24 (Original) The method of claim 23 wherein said base substrate is selected from the group consisting of single crystal silicon, diamond, crystalline oxides, aluminum nitride, other crystalline or amorphous nitrides, amorphous or glassy oxides, plastics, and organic-inorganic composites.

Claim 25 (Original) The method of claim 14 wherein said at least partially crystalline porous layer is selected from the group consisting of at least one porous silicon germanium alloy layer ($Si_{1-x}Ge_x$, where $0 < x < 1$ and x may be constant or spatially variable) and at least one porous silicon germanium alloy layer in combination with porous Si.

Claim 26 (Original) A method for forming and detaching a semiconductor device layer comprising the steps of:

forming a semiconductor layer on a first substrate, wherein said first substrate includes a base substrate and an at least partially crystalline porous release layer, and said at least partially crystalline porous release layer includes at least one porous silicon germanium alloy layer ($Si_{1-x}Ge_x$, where $0 < x < 1$ and x may be constant or spatially variable) alone or in combination with at least one porous Si layer; and

detaching said semiconductor layer from said first substrate by breaking apart said porous release layer.

Claim 27 (Currently Amended) A method for detaching a layer from a semiconductor substrate, said layer initially attached to said semiconductor substrate by a porous layer which is broken apart by the steps of:

introducing a fluid including water into the pores of said porous layer; and

freezing said fluid whereby said fluid expands to break apart said porous layer.

Claim 28 (Original) The method of claim 27 wherein said steps are repeated in one or more freeze-thaw cycles.

Claim 29 (Currently Amended) The method of claim 27 wherein said semiconductor substrate is a crystalline semiconductor substrate, and said porous release layer is at least partially crystalline and formed by the steps of anodic etching of said crystalline semiconductor substrate.

Claim 30 (Currently Amended) The method of claim 27 wherein said semiconductor substrate is a crystalline semiconductor substrate, and said porous release layer is at least partially crystalline and formed by the steps of through a patterned mask.

Claim 31 (Withdrawn) An integrated circuit comprising:

a substrate,

an adhesive layer over said substrate,

a semiconductor layer on said adhesive layer, and

at least one semiconductor device in said semiconductor layer, said semiconductor device formed in said semiconductor layer prior to bonding said semiconductor layer to the said adhesive layer.

Claim 32 (Withdrawn) The integrated circuit structure of claim 31 further including a porous layer below said semiconductor layer.

Claim 33 (Withdrawn) The integrated structure of claim 31 wherein said at least one semiconductor device is selected from the group consisting of n-type metal-oxide-semiconductor devices (NMOS), p-type MOS (PMOS) devices, complementary MOS (CMOS) devices, bipolar transistors, bipolar and CMOS (BiCMOS) devices.

Claim 34 (Withdrawn) The integrated structure of claim 31 wherein said at least one semiconductor device further includes insulating regions extending through said semiconductor layer.

Claim 35 (Withdrawn) The integrated structure of claim 31 wherein said semiconductor layer containing at least one semiconductor device further includes additional layers containing interconnection circuitry.

Claim 36 (Withdrawn) The integrated structure of claim 31 wherein said semiconducting layer is selected from the group consisting of silicon, silicon-germanium alloys, silicon-carbon alloys, silicon-germanium alloys containing carbon; the aforementioned materials doped with any element; the aforementioned materials in layered or graded composition combinations; the aforementioned materials in single crystal, polycrystalline, or nanocrystalline form.

Claim 37 (Withdrawn) The integrated structure of claim 31 wherein said semiconductor layer has a thickness in the range from 20 to 1000 nm.

Claim 38 (Withdrawn) The integrated structure of claim 31 wherein said substrate further includes one of passive cooling an active cooling.

Claim 39 (Withdrawn) The integrated structure of claim 31 wherein said substrate is selected from the group consisting of single crystal silicon, diamond, quartz, crystalline oxides, other crystalline or amorphous nitrides, amorphous or glassy oxides, plastics, and organic-inorganic composites.

Claim 40 (Withdrawn) The integrated structure of claim 31 wherein said substrate includes one or more overlayers selected form the group consisting of highly insulating (> 1kΩ-cm) single-crystal Si, highly insulating (>1kΩ-cm) single-crystal silicon germanium, highly insulating (>1kΩ-cm) polycrystalline Si or highly insulating (>1kΩ-cm) polycrystalline silicon germanium, single crystal diamond, polycrystalline diamond; silicon oxide; aluminum oxide, other metal oxides, aluminum nitride, other crystalline or amorphous nitrides, and mixtures thereof.